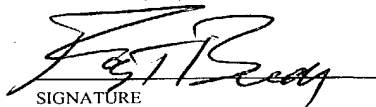


JC10 Rec'd PCT/PTO 15 FEB 2002

FORM PTO-1390 (REV. 11-2000)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 016301-029900US
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371			U.S. APPLICATION NO. (If known, see 37 CFR 1.5) Unknown 10/049689
INTERNATIONAL APPLICATION NO. PCT/US00/22561	INTERNATIONAL FILING DATE 16 August 2000 (16/08/00)	PRIORITY DATE CLAIMED 16 August 1999 (16/08/99)	
TITLE OF INVENTION INTEGRATION SCHEME USING SELF-PLANARIZED DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION			
APPLICANT(S) FOR DO/EO/US GAILLARD, Frederic; GEIGER, Fabrice; YIEH, Ellie			
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:			
<ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371. 2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 36 U.S.C. 371. 3. <input type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f). The submission must include items (5), (6), (9) and (21) indicated below. 4. <input type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31). 5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 37(c)(2)) <ol style="list-style-type: none"> a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> has been communicated by the International Bureau c. <input checked="" type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US). 6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)). <ol style="list-style-type: none"> a. <input type="checkbox"/> is attached hereto. b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4). 7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)). <ol style="list-style-type: none"> a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau). b. <input type="checkbox"/> have been communicated by the International Bureau. c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired. d. <input checked="" type="checkbox"/> have not been made and will not be made. 8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)). 9. <input type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). 10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)). <p>Items 11 to 20 below concern document(s) or information included:</p> <ol style="list-style-type: none"> 11. <input type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98. 12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included. 13. <input type="checkbox"/> A FIRST preliminary amendment. 14. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment. 15. <input type="checkbox"/> A substitute specification. 16. <input type="checkbox"/> A change of power of attorney and/or address letter. 17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825. 18. <input type="checkbox"/> A second copy of the published international application under 36 U.S.C. 19. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4). 20. <input checked="" type="checkbox"/> Other items or information: Transmittal Letter Return Post Card 			

I/S/ Application No. (if known, see 37 CFR 1.5) 10/049689		INTERNATIONAL APPLICATION NO.		ATTORNEY'S DOCKET NUMBER	
21. <input type="checkbox"/> The following fees are submitted:				CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492(A) (1) – (5)):					
Neither international preliminary examination fee (37 CFR 1.492) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO				\$1000.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search report prepared by the EPO of JPO				\$890.00	
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO				\$710.00	
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)				\$690.00	
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)(4)				\$100.00	
ENTER APPROPRIATE BASIC FEE AMOUNT =				\$890.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$130.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	\$	
Total claims	26 - 20 =	6	x \$18.00	\$108.00	
Independent claims	3 - 3 =	0	x \$84.00	\$	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ 280.00	\$	
TOTAL OF ABOVE CALCULATIONS =				\$	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				\$	
SUBTOTAL =				\$	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				\$	
TOTAL NATIONAL FEE =				\$	
Fee for recording the enclosed assignment (37 CFR 1.2(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				\$	
TOTAL FEES ENCLOSED =				\$1128.00	
				Amount to be refunded: \$	
				charged: \$	
a. <input type="checkbox"/> A check in the amount of \$_____ to cover the above fees is enclosed.					
b. <input checked="" type="checkbox"/> Please charge my Deposit Account No. <u>20-1430</u> in the amount of \$ <u>1128.00</u> to cover the above fees.					
c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. <u>20-1430</u> . A duplicate copy of this sheet is enclosed.					
d. <input type="checkbox"/> Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.					
NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO:					
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				Roger T. Barrett NAME	
				41,599 REGISTRATION NUMBER	

15/P-12

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JC11 Rec'd PCT/PTO 15 FEB 2002
PATENT

Attorney Docket No.: AM3299/T29900

TTC No.: 16301-029900

INTEGRATION SCHEME USING SELF-PLANARIZED DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION

BACKGROUND OF THE INVENTION

5 The present invention relates to the fabrication of integrated circuits. More particularly, the present invention is directed toward methods for providing self-planarized deposition of high quality dielectric layers for shallow trench isolation.

 Semiconductor device geometries continue to decrease in size, providing more devices per unit area on a fabricated wafer. These devices are typically initially
10 isolated from each other as they are built into the wafer, and they are subsequently interconnected to create the specific circuit configurations desired. Currently, some devices are fabricated with feature dimensions as small as, or smaller than, 0.18 μm . For example, spacing between devices such as conductive lines or traces on a patterned wafer may be separated by 0.18 μm leaving recesses or gaps of a comparable size. A
15 nonconductive layer of dielectric material, such as silicon dioxide (SiO_2), is typically deposited over the features to fill the aforementioned gaps and insulate the features from other features of the integrated circuit in adjacent layers or from adjacent features in the same layer.

 Dielectric layers are used in various applications including shallow trench
20 isolation (STI) dielectric for isolating devices and interlayer dielectric (ILD) formed between metal wiring layers or prior to a metallization process. In some cases, STI is used for isolating devices having feature dimensions of 0.5 μm or smaller. Planarization of dielectric layers has become increasingly important as the packing densities of semiconductor devices continue to grow.

25 The planarization issue is described using an example of a typical process for forming a shallow trench isolation (commonly referred to as STI integration) as illustrated in Figs. 1A-1G. In Fig. 1A, a silicon substrate 110 has deposited thereon a pad oxide layer 112 and a nitride layer 114 such as silicon nitride. The nitride layer 114 is typically deposited by low pressure chemical vapor deposition (LPCVD), and serves as
30 an etch stop for chemical mechanical polishing (CMP). Referring to Fig. 1B, a bottom anti-reflective coating (BARC) 116 is formed above the nitride layer 114 for absorbing light reflected from the substrate 110 during photolithography. Typically an organic spin-

on glass (SOG), the BARC 116 is needed typically for light having wavelengths of below about 248 nm, including deep ultraviolet (DUV) and far ultraviolet (FUV) light. A photoresist 118 is formed over the BARC 116 and exposed using a mask (not shown) which defines the location of the trenches. The exposed photoresist is then stripped to
5 leave open areas for forming the trenches. Typically, a plasma etch is performed to etch the open areas through the nitride 114, pad oxide 112, and silicon substrate 110 to form the trenches 120, as shown in Fig. 1C. After the remaining photoresist 118 and BARC 116 are removed, a thermal oxide 122 is typically grown on the nitride/pad oxide and on the surfaces of the trenches 120 (trench bottom 124 and trench wall 126) to repair the
10 plasma damage to the silicon substrate 110, as illustrated in Fig. 1D.

A dielectric layer 128 is then deposited over the thermal oxide 122 to fill the trenches 120 and cover the nitride layer 114. This dielectric layer 128 is often referred to as a trench oxide filling layer. Typical dielectric layers are formed from oxide materials such as silicon dioxide or silicate glass. As shown in Fig. 1E, the surface
15 profile of the deposited dielectric layer 128 is stepped and generally resembles the shape of the trenched substrate 110. The surface profile is more uniform in dense fields with closely space narrow trenches than in open fields with wide trenches. As seen in Fig. 1E, a step height 130 is formed in the dielectric profile between the dense field 134 and the open field 132. Because of the step height 130, it is not practicable to apply CMP directly
20 after the dielectric layer deposition step to planarize the dielectric layer 128 because otherwise a dishing effect in the open field 132 will result with CMP, as seen in Fig. 1H. Instead, a reverse mask and etch procedure is used to etch the extra oxide to obtain a more planar surface profile as illustrated in Fig. 1F. This procedure typically involves the steps of photoresist deposit, reverse masking, cure, etched photoresist removal, etchback, and
25 removal of remaining photoresist. A CMP procedure is then applied to the structure of Fig. 1F to globally planarize the surface of the filled substrate 110 as shown in Fig. 1G. The reverse mask and etch procedure necessitated by the step height effect adds significant cost and complexity (for example, due to the added lithography steps involved) to the planarization procedure.

30 From the discussion above, it is seen that multiple steps, including additional photolithography steps (which require expensive equipment), are needed to provide STI. However, it is desirable to reduce the number of steps (and related equipment, especially photolithography equipment which requires expensive lenses, light sources, etc.) and to obtain improved results in order to provide a more economic and

efficient manufacturing process. For example, one way to obtain improved results is to provide a self-planarized, high quality trench oxide filling layer at a reduced cost.

A number of procedures are known for depositing dielectric layers such as the gap-fill dielectric 128 for the trench oxide filling layer in the example shown in Fig.

5 1E. One type of process employs O_3 (ozone) and TEOS (tetraethylorthosilicate) for depositing a dielectric film such as silicate glass. Such films deposited are commonly referred to as " O_3 /TEOS films". O_3 /TEOS processes have a surface sensitivity which increases as the O_3 /TEOS ratio increases. Due to the surface sensitivity, the dielectric deposition rate varies in accordance with the properties of the material of the underlying
10 layer.

It is known to minimize the surface sensitivity by depositing a surface insensitive barrier layer prior to the O_3 /TEOS film deposition. One known method is to lower the surface sensitivity by decreasing the O_3 /TEOS ratio and/or decreasing the pressure. However, lowering the O_3 /TEOS ratio tends to undesirably result in a more
15 porous dielectric film. This is particularly problematic when the dielectric film is used for isolation purposes. One way to address this concern has been to raise the process temperature to above about 500 degrees Celsius, but raising the process temperature is often undesirable. Alternatively, an additional anneal process after the deposition of the trench oxide filling layer has been used to densify the trench oxide filling layer. This
20 method, however, suffers from the need to perform an extra step.

Instead of minimizing the surface sensitivity, some have utilized the deposition rate dependence of O_3 /TEOS films to perform gap fill for a trenched silicon substrate wherein the side walls of the trench are covered with thermal oxide spacers. Using an atmospheric pressure CVD (APCVD) O_3 /TEOS deposition and an ozone
25 concentration of 5%, it was reported that faster film growth on the bottom silicon than on the side wall spacers precluded void formation to achieve void-free gap fill. Others have investigated the feasibility of forming a planarized intermetal dielectric (IMD) by taking advantage of the surface sensitivity of O_3 /TEOS and similar materials such as O_3 -octamethylcyclotetrasiloxane (OMTC). Researchers have reported difficulties of
30 controlling the different deposition rates to achieve planarity. For instance, significant elevations have been observed at the edges of aluminum metal lines caused by the different deposition rates of the O_3 /TEOS on a TiN ARC layer on top of the aluminum and the aluminum side walls. Some of these same researchers have reported more

satisfactory planarization results for depositing SiO₂ layers on an aluminum interconnect built upon a phosphorus glass (PSG) level using O₃-OMTC.

In investigating sub atmospheric chemical vapor deposition (SACVD) of TEOS/O₃ for self-planarized shallow trench isolation (STI) applications, the inventors
5 also encountered difficulties in trench fill quality. As shown in Fig. 2A, porous regions
140 developed in the trench fill dielectric generally adjacent the nitride layer. It is
believed these regions 140 were caused by faster deposition rates (up to 5 times faster) of
TEOS/O₃ on the silicon substrate (i.e., the trench bottom and walls) than on nitride layer
114.

10 After CMP of nitride layer 114 and pad oxide 112, the trench fill material
128 is undercut near the trench corners as shown in Fig. 2B. The eroded trench corners
142 may lead to an undesirable electrostatic field between adjacent active regions
notwithstanding the underlying STI.

What is needed are more efficient and economic methods for self-
15 planarized deposition of a high quality trench oxide filling layer for shallow trench
isolation integration. Improved methods of effectively utilizing the deposition rate
dependence of dielectric materials such as O₃/TEOS films are also desired. It also would
be desirable to provide self-planarized STI without the corner erosion problems depicted
in Fig. 2.

SUMMARY OF THE INVENTION

Specific embodiments of the present invention provide more efficient
methods for providing shallow trench isolation integration by forming self-planarized,
high quality trench fill layers using surface sensitive dielectric materials. The invention
25 does so by depositing a polysilicon layer prior to etching the isolation trenches. The
polysilicon layer moves the porous regions of subsequently deposited trench fill materials
away from the trench, thereby improving trench fill quality. An optional trench cleaning
step can be used prior to deposition to further improve the quality of the trench fill layers
and the electrical characteristics of the device.

30 One embodiment of the invention is directed to a method for forming a
trench isolation structure on a substrate. The method includes applying a pad oxide layer
on the substrate, applying a polysilicon layer over the pad oxide layer, and applying a
CVD anti-reflective coating (ARC) over the polysilicon layer. A photoresist is formed on
the CVD ARC. A portion of the photoresist then is exposed to a light to define a location

where a trench is to be formed, and the photoresist is removed at that location. The method includes etching, at the location, through the CVD ARC, polysilicon layer, pad oxide and through a depth of the substrate to form a trench having a trench bottom.

5 In one aspect, the trench then is filled by introducing a precursor into a substrate processing chamber containing the substrate and flowing ozone into the substrate processing chamber to react with the precursor to deposit a dielectric layer over the substrate. An ozone/precursor ratio is adjusted to regulate deposition rates of the dielectric layer on the trench bottom and the CVD ARC until the dielectric layer develops a substantially planar dielectric surface. In still another aspect, the substrate is subjected
10 to an oxygen-containing gas and heated to substantially simultaneously densify the dielectric layer and to form a thermal oxide at an interface between the dielectric layer and a surface of the trench.

According to yet another embodiment, a method for forming a trench
isolation structure on a substrate includes the step of applying a pad oxide layer on the
15 substrate, applying a polysilicon layer over the pad oxide layer, and applying a nitride layer over the polysilicon layer. A bottom anti-reflective coating (BARC) is applied over the polysilicon layer and a photoresist is formed on the BARC. A portion of the photoresist is exposed to a light to define a location where a trench is to be formed. The photoresist is removed at the location. The method further includes the step of etching, at
20 the location, through the BARC, the nitride layer, the polysilicon layer, the pad oxide and through a depth of the substrate to form a trench at the location.

For a further understanding of the objects and advantages of the present invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

25

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1H are side cross-sectional views of a substrate demonstrating trench formation and trench fill by a dielectric material employing prior art deposition methods;

30 Figs. 2A and 2B depict side cross-sectional views of trenches having undesirable porous regions before and after CMP;

Figs. 3A and 3B are flow diagrams of alternate embodiments of the method of forming a trench in accordance with the present invention;

Figs. 4A and 4B are side cross-sectional views of alternate embodiments of a trenched substrate according to the present invention;

Fig. 5 is a flow diagram of an embodiment of the method of forming a self-planarized trench fill layer formed in accordance with the present invention;

5 Figs. 6A and 6B are side cross-sectional views of alternate embodiments of a substrate with a self-planarized trench fill layer in accordance with the present invention;

Fig. 7 is a flow diagram of an embodiment of the method of processing a trench fill layer in accordance with the present invention;

10 Figs. 8A and 8B are side cross-sectional views of the substrates of Figs. 6A and 6B, respectively, which have been processed with an oxidizing anneal in accordance with the present invention;

Figs. 9A and 9B are side cross-sectional views of the substrates of Figs. 8A and 8B, respectively, after a planarization step in accordance with the present invention;

Fig. 10 is a side cross-sectional view of one embodiment of a chemical vapor deposition apparatus according to the present invention;

Figs. 11 and 12 are exploded perspective views of parts of the CVD chamber depicted in Fig. 10; and

20 Fig. 13 is a simplified diagram of system monitor and CVD system in a multichamber system, which may include one or more chambers.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

I. Self-Planarized Deposition of a Dielectric Layer in Shallow Trench Integration

25 Specific embodiments of the present invention are illustrated using an STI integration as an example. The benefits of the various embodiments of the invention can be readily seen by comparison with the prior art methods, such as illustrated in Figs. 1A-1H. Specifically, the present invention provides more efficient shallow trench isolation integration by providing self-planarized deposition of a dielectric trench fill layer without sacrificing the quality of the dielectric layer. The present invention further provides dielectric trench fill layers which have undesirable porous regions removed by CMP. It is understood that the scope of the invention is not necessarily limited to STI integration.

A. Forming a Trench

Figs. 3A and 3B illustrate alternate methods of forming a trench on a substrate, typically a silicon substrate. Referring to Fig. 3A, the first step 202 is to apply a pad oxide directly on the silicon substrate. In one particular embodiment, pad oxide is about 60 Angstroms (\AA) thick, although other thicknesses may be used. Pad oxide operates to protect the underlying substrate, particularly from stresses caused by subsequently deposited nitride layers. Next, a polysilicon layer is deposited over the pad oxide layer in step 204. In one embodiment, polysilicon layer is about 400\AA - 1000\AA thick, and in one particular embodiment is about 600\AA thick. The purpose and function of the polysilicon layer is described in further detail below. Step 210 is to apply a CVD anti-reflective coating (CVD ARC) directly to the polysilicon layer. Unlike the commonly used organic spin on BARC, CVD ARC is an inorganic material that typically includes, for example, silicon nitride, silicon oxynitride, or silicon carbide. The CVD ARC is deposited by promoting chemical reaction of the process gases in a CVD system. For example, a CVD ARC which includes silicon, and nitrogen and/or oxygen (also known as a dielectric ARC or DARC) is deposited by introducing the following process gases in plasma-enhanced CVD (PECVD): a silicon-containing gas (such as silane or TEOS), and a nitrogen-containing gas and/or an oxygen-containing gas. Nitrous oxide (N_2O) may be used for supplying nitrogen and oxygen, but other sources of oxygen and nitrogen can of course be used. An inert gas such as helium or argon is typically used for controlling the deposition rate of the process and the film thickness, and for stabilizing the process.

An example of a suitable CVD apparatus is described in U.S. Patent No. 5,558,717 entitled "CVD PROCESSING CHAMBER," issued to Zhao et al. The gas ratio can be adjusted to obtain a film composition with the desired optical characteristics (refractive index and absorptive index) of the deposited CVD ARC. A CVD ARC silicon nitride layer differs from the conventional LPCVD silicon nitride layer in that the film composition of the LPCVD silicon cannot be modified because LPCVD is a thermal process rather than a plasma-enhanced process. Some of the techniques that can be used to deposit CVD ARC are described in U.S. Patent Application No. 08/672,888 entitled "METHOD AND APPARATUS FOR DEPOSITING ANTIREFLECTIVE COATING," having David Cheung, Joe Feng, Judy H. Huang, and Wai-Fan Yau as inventors; U.S. Patent Application No. 08/852,787 entitled "METHOD AND APPARATUS FOR DEPOSITING AN ETCH STOP LAYER," having Judy H. Huang, Wai-Fan Yau, David Cheung, and Chan-Lon Yang as inventors; and "Novel ARC Optimization Methodology

for KrF Excimer Laser Lithography at Low K1 Factor" by Tohru Ogawa, Mitsunori Kimura, Yoichi Tomo, and Toshiro Tsumori, published in the SPIE Proceedings (Optical/Laser Microlithography V), Volume 1674, pages 362-375 (1992). The two applications are assigned to Applied Materials, Inc., the assignee of the present invention.

5 Each of these references are incorporated herein by reference.

In one embodiment, a desired ratio of silane (SiH_4) to N_2O is selected for depositing a DARC. In addition, N_2 and NH_3 are introduced to further control the optical and chemical properties of the DARC deposited. The effects of N_2 and NH_3 are particularly dominant in process regimes where SiH_4 and N_2O have minimal or no effect
 10 on the DARC properties, e.g., at low temperature. The addition of NH_3 and N_2 in the process further changes the composition of the film, allowing more freedom and finer tuning of the refractive index and the absorptive index. Furthermore, the process is compatible with the use of helium, which is more cost-effective than argon. Helium also allows for improved stress control of the DARC layer deposited. This helps prevent the
 15 film from becoming too tensile, which can cause it to flake off the substrate after deposition.

The CVD ARC has the ability to absorb light reflected from the substrate during photolithography similar to the BARC (Fig. 1B). In addition, the CVD ARC has a reflective property that allows it to reflect light that is out-of-phase from light reflected
 20 from the substrate so that the two cancel each other in what is referred to as a phase shift cancellation. The CVD ARC serves photolithography and, if desired, CMP purposes. CVD ARC also is a good barrier to oxygen diffusion. In one particular embodiment, the CVD ARC is used as an etch stop for CMP, making it possible to eliminate the LPCVD nitride layer (Fig. 1G), as mentioned above.

Referring again to Fig. 3A, a photoresist is formed over the CVD ARC at
 25 step 212. The photoresist is exposed to define the trench location where the trench is to be formed (step 214) and the exposed photoresist is then stripped at the trench location (step 216) according to a specific embodiment. An etching step 218 is performed to etch the CVD ARC, the polysilicon layer, pad oxide and silicon substrate to form the trench at
 30 the trench location. At step 220, the remaining photoresist is removed. According to some specific embodiments, an optional clean step 222 can be performed to clean the trench and remove contaminants. The clean step 222 can employ, for example, a conventional wet etching procedure using a mixture containing hydrofluoric acid (HF). The resultant structure is illustrated in Fig. 4A, which shows the silicon substrate 224

with, a pad oxide 226 and a polysilicon layer 228 formed thereon. In one embodiment, pad oxide 226 is about 60Å thick, and polysilicon layer 228 is about 600Å thick, although other thicknesses may be used. A CVD ARC 230 overlying polysilicon layer 228 has a thickness of about 1000-2000 Å. The formed trench 232 has a trench bottom and a trench wall 234.

Compared with the conventional approach illustrated in Figs. 1A-1D, the method of Fig. 3A can eliminate the process of growing a thermal oxide over the surfaces of the trench, which is conventionally used to repair the plasma damage to the silicon substrate during trench formation. The inventors have found that depositing the surface sensitive dielectric material such as O₃/TEOS directly over a silicon trench significantly improves the quality of the trench fill layer to be formed over prior approaches and that the clean step 222 can further improve film quality, as discussed in more detail below. In addition, the inventors have discovered that an oxidizing anneal process can be used after formation of the trench fill layer to grow a thermal oxide at the trench bottom and trench wall as discussed below.

In an alternate embodiment shown in Fig. 3B, steps 250 and 252 are the same as steps 202 and 204, respectively. After the polysilicon layer is deposited, a nitride layer, such as LPCVD nitride, is applied over the polysilicon (step 254) and BARC is applied over the nitride layer (step 256). In this embodiment, an additional polysilicon layer is deposited compared to the method depicted in Figs. 1A-1C. Thereafter, steps 258-268 are the same as steps 212-222 of Fig. 3A and are carried out to etch the trench using the photoresist.

The resultant structure is illustrated in Fig. 4B, which shows a silicon substrate 270 with a pad oxide 272, a polysilicon layer 274, a nitride layer 276 and BARC 278 formed thereon. A trench 280 is etched through layers 272-278 and into silicon substrate 270, defining a trench bottom and a trench wall 282. In contrast to Fig. 1D, thermal oxide is not grown at this stage. A subsequent anneal step operates to form thermal oxide along trench wall 282.

Thereafter, a clean step 266 is advantageously performed using a conventional wet etching process with an HF mixture or the like to remove contaminants. As discussed below, the inventors have discovered that this clean step 266 improves the quality of the trench fill layer that will be deposited. BARC 278 is removed prior to trench fill.

The CVD ARC may be used in specific embodiments of the invention. According to some specific embodiments, subsequent process steps described below may be used whether the CVD ARC/polysilicon/oxide or the BARC/nitride/polysilicon/oxide combination is used. Therefore, after the formation of the trench, the term "etch stop" layer will be used instead and is understood to represent an LPCVD nitride layer or CVD ARC.

B. Depositing a Trench Fill Layer

Referring to Fig. 5, after the trenched substrate (224 in Fig. 4A or 270 in Fig. 4B) is prepared, it is placed in a process chamber (such as the chamber 15 of Fig. 10) in step 290. Typically an inert gas is flowed into the chamber in step 292 to stabilize the pressure in the chamber before reactive process gases are introduced. Next, a precursor having a surface sensitivity and growth rate dependence on differently constituted surfaces is introduced into the chamber (step 294). An example of a suitable precursor is TEOS. Because TEOS is a liquid precursor, a suitable apparatus directs the bubbling of a delivery gas, such as helium, through the TEOS in a bubbler assembly or introducing a carrier gas, such as helium or nitrogen, to a liquid injection system to vaporize the TEOS and form a process gas having the desired flow rates. An ozone gas is flowed into the chamber (step 296) to react with the TEOS to deposit an O₃/TEOS trench fill layer over the substrate. The deposition rate of the O₃/TEOS layer is faster on the lower trench bottom (which is silicon) than on the higher surfaces of the upper portions of the substrate that include the etch stop layer (which is CVD ARC for Fig. 4A and nitride for Fig. 4B). For example, deposition of O₃/TEOS layer on silicon and polysilicon proceed at about the same rate. This deposition rate is as much as five times greater than the rate on nitride, for example on the nitride layer in Fig. 4B and CVD ARC in Fig. 4A.

The relative deposition rates of the O₃/TEOS layer on the lower and higher surfaces are regulated in step 298 by adjusting the O₃/TEOS ratio until the O₃/TEOS layer develops a substantially self-planarized dielectric surface. The O₃/TEOS ratio can be adjusted by adjusting the flow rates of the O₃ and/or TEOS. For instance, a predetermined O₃/TEOS ratio can be selected and the relative flow rates are adjusted to achieve that ratio in step 298. It is advantageous to maximize the O₃/TEOS ratio to accelerate the deposition from the trench bottom to achieve planarity. O₃/TEOS ratios of desirably higher than about 10:1, and more desirably about 10:1 to 20:1, can be used.

The deposition of the trench fill layer can take place at a relatively low temperature of under about 500°C, for example about 300-500°C. This advantageously avoids the undesirable aluminum fluoride formation which may occur when deposition occurs at high temperatures above about 500°C in processing chambers that include aluminum materials and the longer cleaning time required to remove the aluminum fluoride. Other process parameters such as pressure and flow rates can be adjusted to optimize the deposition process for a selected O₃/TEOS ratio. A pressure ranging from about 200 to 700 Torr is preferable for use with O₃/TEOS ratios of 10:1 to 20:1.

Figs. 6A and 6B illustrate the self-planarized trench fill dielectric layers 300 and 304, respectively, deposited over the substrates 224, 270 of Figs. 4A and 4B. While the variance in deposition rates of O₃/TEOS due to the underlying surface is used advantageously to create a substantially self-planarized STI structure, trench fill quality issues arise. More specifically, porous regions 302, 306 tend to form adjacent the nitride layer due at least in part to the slower deposition rate thereon. These porous regions lead to the problems discussed in conjunction with Fig. 2. At least part of the present invention is the recognition that the use of polysilicon layers 228, 274 elevate the porous regions away from the trench openings, and hence away from the trench corners. The use of polysilicon is advantageous at least in part due to the similar deposition rates of O₃/TEOS on polysilicon and silicon. Further advantages of using polysilicon also are realized in the subsequent anneal process described in conjunction with Figs. 7 and 8.

Hence, the present methods not only provide self-planarized deposition of the trench fill layers, but also ensure that these layers are of high quality.

C. Processing the Trench Fill Layer

Referring to Fig. 7, steps 310 and 312 represent an oxidizing anneal process that can be used to grow a thermal oxide at the trench surfaces after the trenches have been filled with the deposited trench fill layer. Further details may be found in European Patent Application No. 98401232, entitled METHODS FOR FORMING SELF-PLANARIZED DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION, filed May 22, 1998, and assigned to the assignee of the present invention, the complete disclosure of which is incorporated herein by reference. While the process has general applicability beyond the STI integration described herein, it has particular advantages in this example because the prior thermal oxide growth (Fig. 1D) has been eliminated to

ensure formation of a high quality trench fill layer (e.g., O_3 /TEOS) and global planarization in the method of Figs. 3A and 3B. This subsequent oxidizing anneal not only causes a thermal oxide to grow at the trench surfaces, but it substantially simultaneously densifies the trench fill layer, further improving its quality. A dense layer is advantageous, particularly for isolation purposes.

The oxidizing anneal is performed by subjecting the substrate to an oxygen-containing gas in step 310 (such as molecular oxygen, steam, and any precursor with oxygen); and heating the substrate to a suitable temperature (e.g., above about 800°C) in step 312. In one particular embodiment, the substrate is heated to about 1050°C in a 100% O_2 atmosphere for about 40 minutes. In another embodiment, the substrate is heated to about 850°C in an atmosphere comprising 60% H_2O and 40% nitrogen for about 30 minutes.

As the substrates 224 and 270 of Figs. 6A and 6B, respectively, undergo the oxidizing anneal, a thermal oxide 307 and 309 is grown along the surfaces of the trench 232 and 280 as illustrated in Figs. 8A and 8B. The oxidizing anneal is desirably made before CMP to improve the CMP process, because the surface sensitive deposition is more porous on active areas (LPCVD nitride or CVD ARC) than on the trenches (silicon) as deposited. This difference in film density can be beneficial for the CMP process since the CMP rate will be higher over the active area than over the trenches.

A further advantage of polysilicon is the oxidation rate thereof is about two times as great as that for silicon. As shown in Figs. 8A and 8B, thermal oxide 307, 309 is approximately twice as thick along the polysilicon layer compared to along the silicon trench surfaces. In this manner, the polysilicon oxidation provides exemplary trench corners of trench fill material.

The final step 314 is to selectively remove and planarize the trench fill material, typically by CMP. This step removes the trench fill material over the etch-stop layer which can be the nitride layer or CVD ARC. Because the dielectric profile is substantially planar, no reverse mask and etch procedure is necessary and the CMP step can be completed more quickly than the case where the dielectric profile is stepped, such as that shown in Fig. 1F. This further decreases process time and increases throughput.

Further, the use of polysilicon layers 228, 274 have elevated porous regions 302, 306 to be further away from the trench openings. As shown in Figs. 9A and 9B, CMP removes porous regions 302, 306, thereby increasing the consistency of the

remaining trench fill dielectric layers 300, 304. Further, exemplary trench corner fill is provided to help avoid electrostatic field over the trench. Hence, problems discussed in conjunction with Fig. 2 are avoided.

5 II. An Exemplary CVD System

Fig. 10 depicts one suitable CVD apparatus in which at least portions of the methods of the present invention can be carried out. For example, deposition steps, including deposition of pad oxide, nitride, BARC, CVD ARC, and trench fill dielectrics may be carried out in the system of Fig. 10, or similar systems. Conventional systems
10 known to those skilled in the art may be used for polysilicon deposition, and performing photoresist, etching, and CMP processes in accordance with the present invention.

Fig. 10 shows a vertical, cross-sectional view of a CVD system 10, having a vacuum or processing chamber 15 that includes a chamber wall 15a and chamber lid assembly 15b. Chamber wall 15a and chamber lid assembly 15b are shown in exploded, perspective views in Figs. 11 and 12. CVD system 10 contains a gas distribution
15 manifold 11 for dispersing process gases to a substrate (not shown) that rests on a heated pedestal 12 centered within the process chamber. During processing, the substrate (e.g. a semiconductor wafer) is positioned on a flat (or slightly convex) surface 12a of pedestal 12. The pedestal can be moved controllably between a lower loading/off-loading position
20 (not shown) and an upper processing position (shown in Fig. 10), which is closely adjacent to manifold 11. A centerboard (not shown) includes sensors for providing information on the position of the wafers.

Deposition and carrier gases are introduced into chamber 15 through perforated holes 13b (Fig. 12) of a conventional flat, circular gas distribution or faceplate
25 13a. More specifically, deposition process gases flow into the chamber through the inlet manifold 11 (indicated by arrow 40 in Fig. 10), through a conventional perforated blocker plate 42 and then through holes 13b in gas distribution faceplate 13a.

Before reaching the manifold, deposition and carrier gases are input from gas sources 7 through gas supply lines 8 (Fig. 10) into a mixing system 9 where they are
30 combined and then sent to manifold 11. Generally, the supply line for each process gas includes (i) several safety shut-off valves (not shown) that can be used to automatically or manually shut-off the flow of process gas into the chamber, (ii) mass flow controllers (also not shown) that measure the flow of gas through the supply line, and (iii) gas delivery line heating to prevent, for example, liquid condensation therein. When toxic

gases (for example, ozone or halogenated gas) are used in the process, the several safety shut-off valves are positioned on each gas supply line in conventional configurations.

The deposition process performed in CVD system 10 can be either a thermal process or a plasma-enhanced process. In a plasma-enhanced process, an RF power supply 44 applies electrical power between the gas distribution faceplate 13a and the pedestal so as to excite the process gas mixture to form a plasma within the cylindrical region between the faceplate 13a and the pedestal. (This region will be referred to herein as the "reaction region"). Constituents of the plasma react to deposit a desired film on the surface of the semiconductor wafer supported on pedestal 12. RF power supply 44 is a mixed frequency RF power supply that typically supplies power at a high RF frequency (RF1) of 13.56 MHz and at a low RF frequency (RF2) of 360 KHz to enhance the decomposition of reactive species introduced into the vacuum chamber 15. In a thermal process, RF power supply 44 would not be utilized, and the process gas mixture thermally reacts to deposit the desired films on the surface of the semiconductor wafer supported on pedestal 12, which is resistively heated to provide thermal energy for the reaction.

During a plasma-enhanced deposition process or thermal process, a liquid is circulated through the walls 15a of the process chamber to maintain the chamber at a desired temperature, e.g., about 65 degrees Celsius. Fluids used to maintain the chamber walls 15a include the typical fluid types, i.e., water-based ethylene glycol or oil-based thermal transfer fluids. Maintaining the wall temperature beneficially reduces or eliminates condensation of undesirable reactant products and improves the elimination of volatile products of the process gases and other contaminants that might contaminate the process if they were to condense on the walls of cool vacuum passages and migrate back into the processing chamber during periods of no gas flow.

The remainder of the gas mixture that is not deposited in a layer, including reaction products, is evacuated from the chamber by a vacuum pump (not shown). Specifically, the gases are exhausted through an annular, slot-shaped orifice 16 surrounding the reaction region and into an annular exhaust plenum 17. The annular slot 16 and the plenum 17 are defined by the gap between the top of the chamber's cylindrical side wall 15a (including the upper dielectric lining 19 on the wall) and the bottom of the circular chamber lid 20. The 360° circular symmetry and uniformity of the slot orifice 16 and the plenum 17 are important to achieving a uniform flow of process gases over the wafer so as to deposit a uniform film on the wafer.

From the exhaust plenum 17, the gases flow underneath a lateral extension portion 21 of the exhaust plenum 17, past a viewing port (not shown), through a downward-extending gas passage 23, past a vacuum shut-off valve 24 (whose body is integrated with the lower chamber wall 15a), and into the exhaust outlet 25 that connects to the external vacuum pump (not shown) through a foreline (also not shown).

The wafer support platter of the pedestal 12 (preferably aluminum, ceramic, or a combination thereof) is resistively-heated using an embedded single-loop embedded heater element configured to make two full turns in the form of parallel concentric circles. An outer portion of the heater element runs adjacent to a perimeter of the support platter, while an inner portion runs on the path of a concentric circle having a smaller radius. The wiring to the heater element passes through the stem of the pedestal 12.

Typically, any or all of the chamber lining, gas inlet manifold faceplate, and various other reactor hardware are made out of material such as aluminum, anodized aluminum, or ceramic. An example of such a CVD apparatus is described in U.S. Patent 5,558,717 entitled "CVD Processing Chamber," issued to Zhao et al. The 5,558,717 patent is assigned to Applied Materials, Inc., the assignee of the present invention, and is hereby incorporated by reference.

A lift mechanism and motor (not shown) raises and lowers the heated pedestal assembly 12 and its wafer lift pins 12b as wafers are transferred into and out of the body of the chamber by a robot blade (not shown) through an insertion/removal opening 26 in the side of the chamber 10. The motor raises and lowers pedestal 12 between a processing position 14 and a lower, wafer-loading position. The motor, valves or flow controllers connected to the supply lines 8, gas delivery system, throttle valve, RF power supply 44, and chamber and substrate heating systems are all controlled by a system controller 34 (Fig. 10) over control lines 36, of which only some are shown. Controller 34 relies on feedback from optical sensors to determine the position of movable mechanical assemblies such as the throttle valve and susceptor which are moved by appropriate motors under the control of controller 34.

In a preferred embodiment, the system controller includes a hard disk drive (memory 38), a floppy disk drive and a processor 37. The processor contains a single-board computer (SBC), analog and digital input/output boards, interface boards and stepper motor controller boards. Various parts of CVD system 10 conform to the Versa Modular European (VME) standard which defines board, card cage, and connector

dimensions and types. The VME standard also defines the bus structure as having a 16-bit data bus and a 24-bit address bus.

System controller 34 controls all of the activities of the CVD machine. The system controller executes system control software, which is a computer program stored in a computer-readable medium such as a memory 38. Preferably, memory 38 is a hard disk drive, but memory 38 may also be other kinds of memory. The computer program includes sets of instructions that dictate the timing, mixture of gases, chamber pressure, chamber temperature, RF power levels, susceptor position, and other parameters of a particular process. Other computer programs stored on other memory devices including, for example, a floppy disk or other another appropriate drive, may also be used to operate controller 34.

The interface between a user and controller 34 is via a CRT monitor 50a and light pen 50b, shown in Fig. 12, which is a simplified diagram of the system monitor and CVD system 10 in a substrate processing system, which may include one or more chambers. In the preferred embodiment two monitors 50a are used, one mounted in the clean room wall for the operators and the other behind the wall for the service technicians. The monitors 50a simultaneously display the same information, but only one light pen 50b is enabled. A light sensor in the tip of light pen 50b detects light emitted by CRT display. To select a particular screen or function, the operator touches a designated area of the display screen and pushes the button on the pen 50b. The touched area changes its highlighted color, or a new menu or screen is displayed, confirming communication between the light pen and the display screen. Other devices, such as a keyboard, mouse, or other pointing or communication device, may be used instead of or in addition to light pen 50b to allow the user to communicate with controller 34.

The above reactor description is mainly for illustrative purposes, and other plasma CVD equipment such as electron cyclotron resonance (ECR) plasma CVD devices, induction coupled RF high density plasma CVD devices, or the like may be employed. Additionally, variations of the above-described system, such as variations in pedestal design, heater design, RF power frequencies, location of RF power connections and others are possible. For example, the wafer could be supported by a susceptor and heated by quartz lamps. The layer and method for forming such a layer of the present invention is not limited to any specific apparatus or to any specific plasma excitation method.

The present method can be used to improve the global planarization while providing exemplary dielectric film quality due in part to the use of a polysilicon layer to move undesirable porous regions away from the trench. The present method further reduces cost and increases throughput. The oxidizing anneal makes it possible to grow a thermal oxide at the trench surfaces after filling the trenches with a self-planarized, high quality trench fill layer. The oxidizing anneal, coupled with the use of the polysilicon layer, provides improved trench fill quality with exemplary trench corners. The use of CVD ARC for photolithography and CMP purposes to form trenches is more efficient and results in a simpler structure. In addition, alternate embodiments can be devised by, for example, varying the O_3 /TEOS ratio, pressure, or other parameters for dielectric deposition.

The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

15

WHAT IS CLAIMED IS:

1 1. A method of forming a trench isolation structure on a substrate, the
 2 method comprising:
 3 applying a pad oxide layer on said substrate;
 4 applying a polysilicon layer over said pad oxide layer;
 5 applying an anti-reflective coating (ARC) over said polysilicon layer;
 6 forming a photoresist on said ARC;
 7 exposing a portion of said photoresist to a light to define a location where
 8 a trench is to be formed;
 9 removing said photoresist at said location; and
 10 etching, at said location, through said ARC, said polysilicon layer, said
 11 pad oxide and through a depth of said substrate to form a trench having a trench bottom at
 12 said location.

1 2. The method of claim 1 further comprising depositing a nitride layer
 2 between said polysilicon layer and said ARC, and wherein said ARC comprises a bottom
 3 anti-reflective coating (BARC).

1 3. The method of claim 1 wherein said ARC comprises a chemical
 2 vapor deposition anti-reflective coating (CVD ARC).

1 4. A method of forming a trench isolation structure on a substrate, the
 2 method comprising:
 3 applying a pad oxide layer on said substrate;
 4 applying a polysilicon layer over said pad oxide layer;
 5 applying a CVD anti-reflective coating (ARC) over said polysilicon layer;
 6 forming a photoresist on said CVD ARC;
 7 exposing a portion of said photoresist to a light to define a location where
 8 a trench is to be formed;
 9 removing said photoresist at said location; and
 10 etching, at said location, through said CVD ARC, said polysilicon layer,
 11 said pad oxide and through a depth of said substrate to form a trench having a trench
 12 bottom at said location.

1 5. The method of claim 4 wherein said polysilicon layer is applied
2 with a thickness of about 400Å to about 1000Å.

1 6. The method of claim 4 wherein said CVD ARC is applied with a
2 thickness of about 1000Å and about 2000Å.

1 7. The method of claim 4 further comprising, following said etching
2 step:
3 removing a remainder of said photoresist; and
4 filling said trench on said substrate with a trench fill material.

1 8. The method of claim 7, wherein said filling step comprises
2 introducing a precursor into a substrate processing chamber containing
3 said substrate;
4 flowing ozone into said substrate processing chamber to react with said
5 precursor to deposit a dielectric layer over said substrate; and
6 adjusting an ozone/precursor ratio between said ozone and said precursor
7 to regulate deposition rates of said dielectric layer on said trench bottom and said CVD
8 ARC until said dielectric layer develops a substantially planar dielectric surface.

1 9. The method of claim 8 wherein said dielectric layer has a ratio of
2 said ozone to said precursor of about 10:1 to 20:1.

1 10. The method of claim 8 wherein said dielectric layer comprises a
2 porous region that is within said trench and generally aligned with said CVD ARC layer.

1 11. The method of claim 8 further comprising:
2 subjecting said substrate to an oxygen-containing gas; and
3 heating said substrate to substantially simultaneously densify said
4 dielectric layer and to form a thermal oxide at an interface between said dielectric layer
5 and a surface of said trench.

1 12. The method of claim 10 further comprising removing a portion of
2 said dielectric layer, including said porous region.

1 13. The method of claim 12 wherein said removing step is a chemical
2 mechanical polishing (CMP) step.

1 14. The method of claim 8 further comprising the step of generating a
2 pressure of about 200-700 Torr and a temperature of about 300-500 degrees Celsius in
3 said substrate processing chamber.

1 15. The method of claim 8 further comprising the step of controlling a
2 pressure in said substrate processing chamber based on an ozone/precursor ratio selected
3 during said adjusting step.

1 16. A method of forming a trench isolation structure on a substrate, the
2 method comprising:
3 applying a pad oxide layer on said substrate;
4 applying a polysilicon layer over said pad oxide layer;
5 applying a nitride layer over said polysilicon layer;
6 applying a bottom anti-reflective coating (BARC) over said polysilicon
7 layer;
8 forming a photoresist on said BARC;
9 exposing a portion of said photoresist to a light to define a location where
10 a trench is to be formed;
11 removing said photoresist at said location; and
12 etching, at said location, through said BARC, said nitride layer, said
13 polysilicon layer, said pad oxide and through a depth of said substrate to form said trench
14 at said location.

1 17. The method of claim 16 wherein said polysilicon layer is applied
2 with a thickness of about 400Å to about 1000Å.

1 18. The method of claim 16 wherein said nitride layer is applied with a
2 thickness of about 800Å to about 1200Å.

1 19. The method of claim 16 further comprising, following said etching
2 step:
3 removing a remainder of said photoresist; and

4 filling said trench on said substrate with a trench fill material.

1 20. The method of claim 19, wherein said filling step comprises
2 introducing a precursor into a substrate processing chamber containing
3 said substrate;
4 flowing ozone into said substrate processing chamber to react with said
5 precursor to deposit a dielectric layer over said substrate; and
6 adjusting an ozone/precursor ratio between said ozone and said precursor
7 to regulate deposition rates of said dielectric layer on said trench bottom and said CVD
8 ARC until said dielectric layer develops a substantially planar dielectric surface.

1 21. The method of claim 19 wherein said dielectric layer comprises a
2 porous region that is proximate a trench wall and is generally aligned with said nitride
3 layer.

1 22. The method of claim 20 further comprising:
2 subjecting said substrate to an oxygen-containing gas; and
3 heating said substrate to substantially simultaneously densify said
4 dielectric layer and to form a thermal oxide at an interface between said dielectric layer
5 and a surface of said trench.

1 23. The method of claim 22 wherein said subjecting and heating steps
2 form said thermal oxide to be about 200Å along a trench wall and about 400Å along said
3 polysilicon layer.

1 24. The method of claim 22 wherein said heating step comprises
2 heating said substrate to between about 800 degrees Celsius and about 1100 degrees
3 Celsius, for about 30-40 minutes.

1 25. The method of claim 21 further comprising removing a portion of
2 said dielectric layer including said porous region.

1 26. The method of claim 21 wherein said removing step is a chemical-
2 mechanical polishing step

INTEGRATION SCHEME USING SELF-PLANARIZED DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION

ABSTRACT OF THE DISCLOSURE

5 A method for forming a trench isolation structure on a substrate. The method includes applying a pad oxide layer (226) on the substrate (224), applying a polysilicon layer (228) over the pad oxide layer, and applying a CVD anti-reflective coating (ARC) (230) over the polysilicon layer. A photoresist is formed on the CVD ARC and a trench is etched at a desired location. One embodiment provides a method for depositing a trench oxide filling
10 layer (300) on the trenched substrate utilizing the surface sensitivity of dielectric materials such as O_3 /TEOS to achieve a substantially self-planarized dielectric layer. Prior problems with porous trench fill, particular near trench corners, are obviated by use of the polysilicon layer. After deposition, an oxidizing anneal can be performed to grow a thermal oxide (307) at the trench surfaces and densify the dielectric material. A chemical mechanical polish can
15 be used to remove the excess oxide material, including the porous regions.

1 / 15

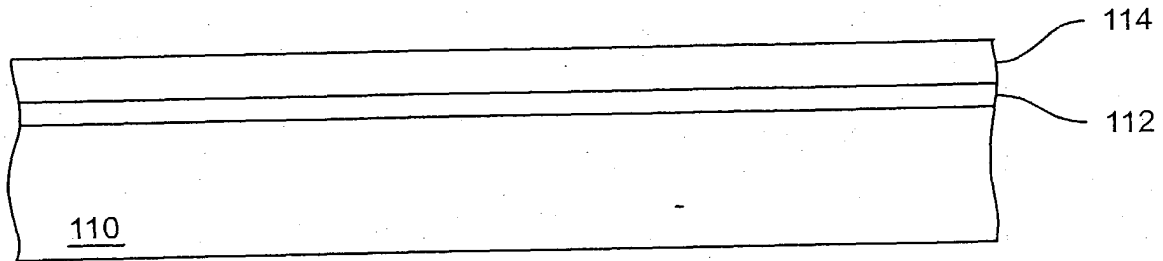


FIG. 1A

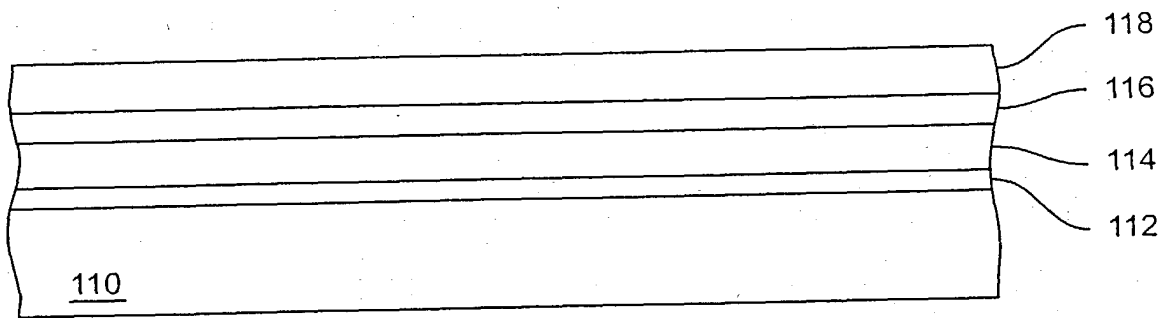


FIG. 1B

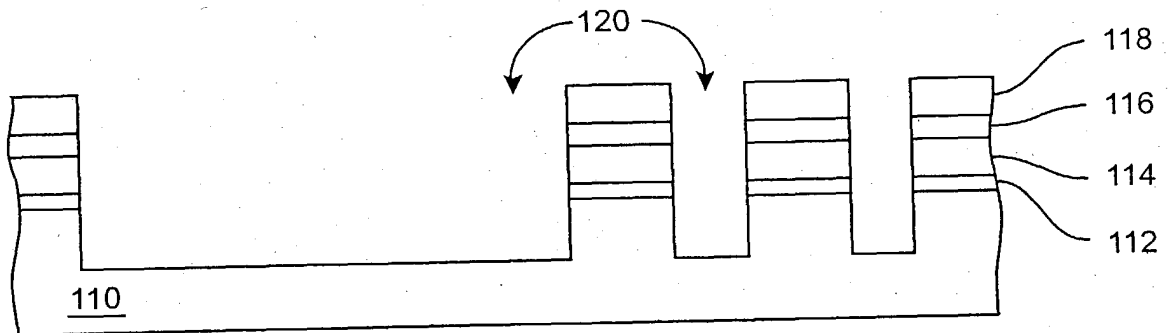


FIG. 1C

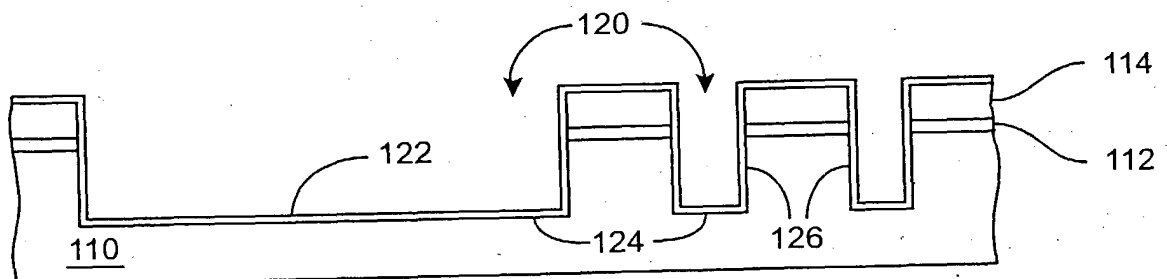


FIG. 1D

2 / 15

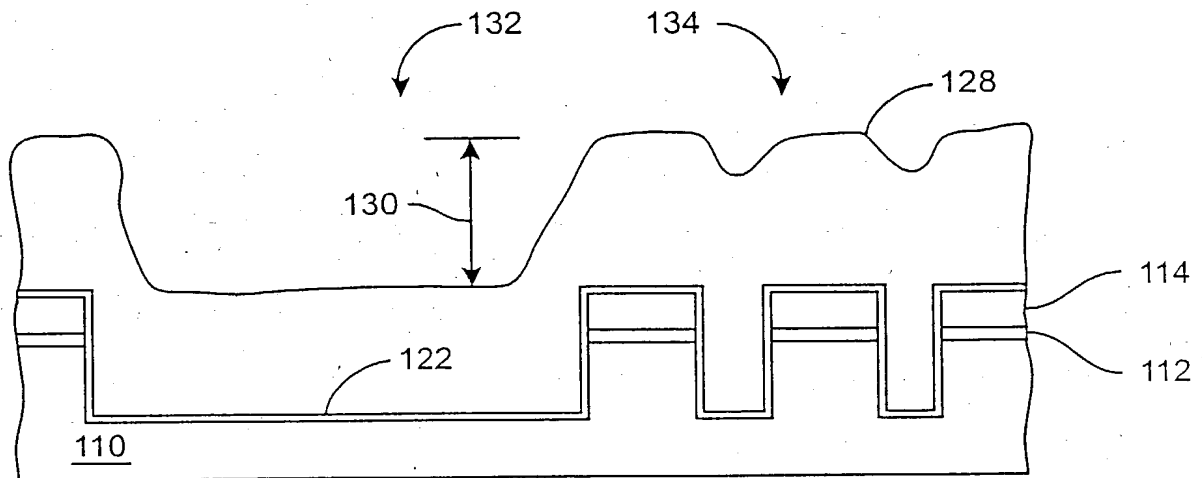


FIG. 1E

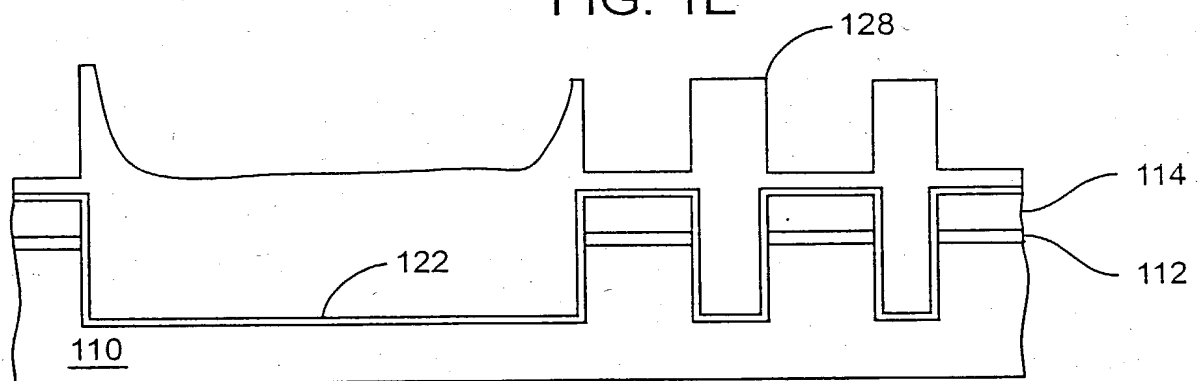


FIG. 1F

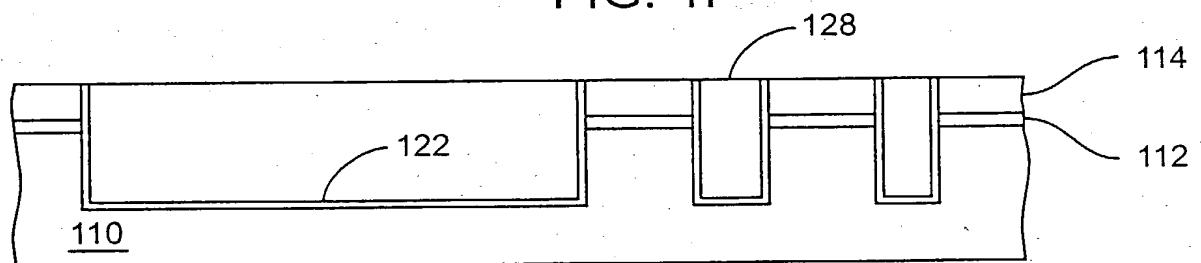


FIG. 1G

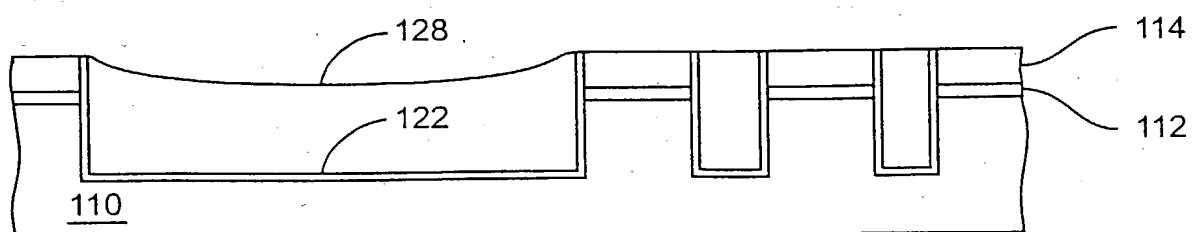


FIG. 1H

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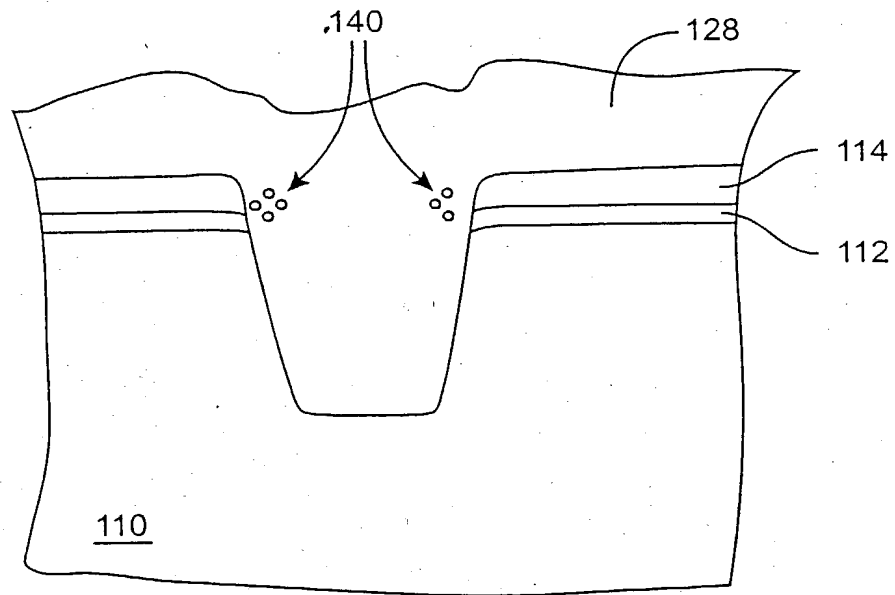


FIG. 2A

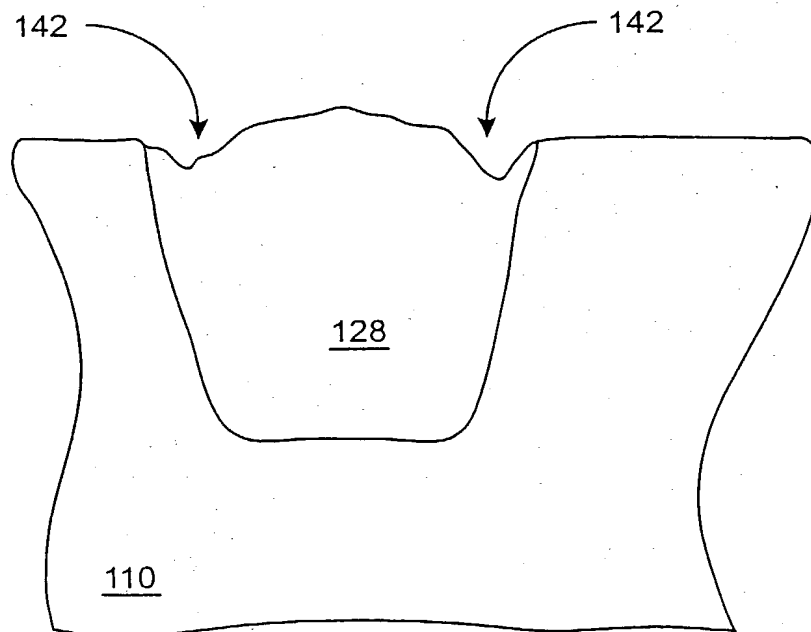


FIG. 2B

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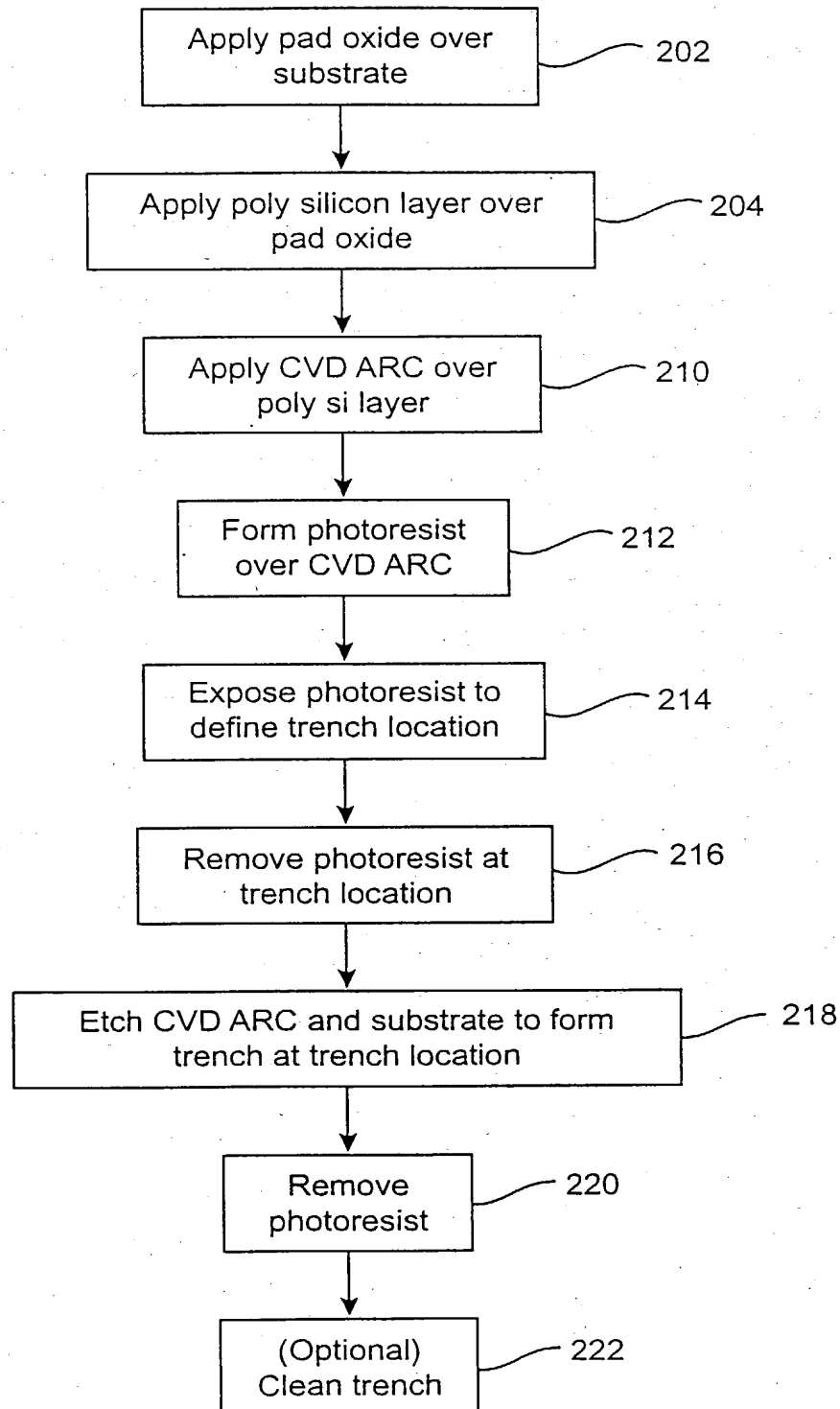


FIG. 3A

5 / 15

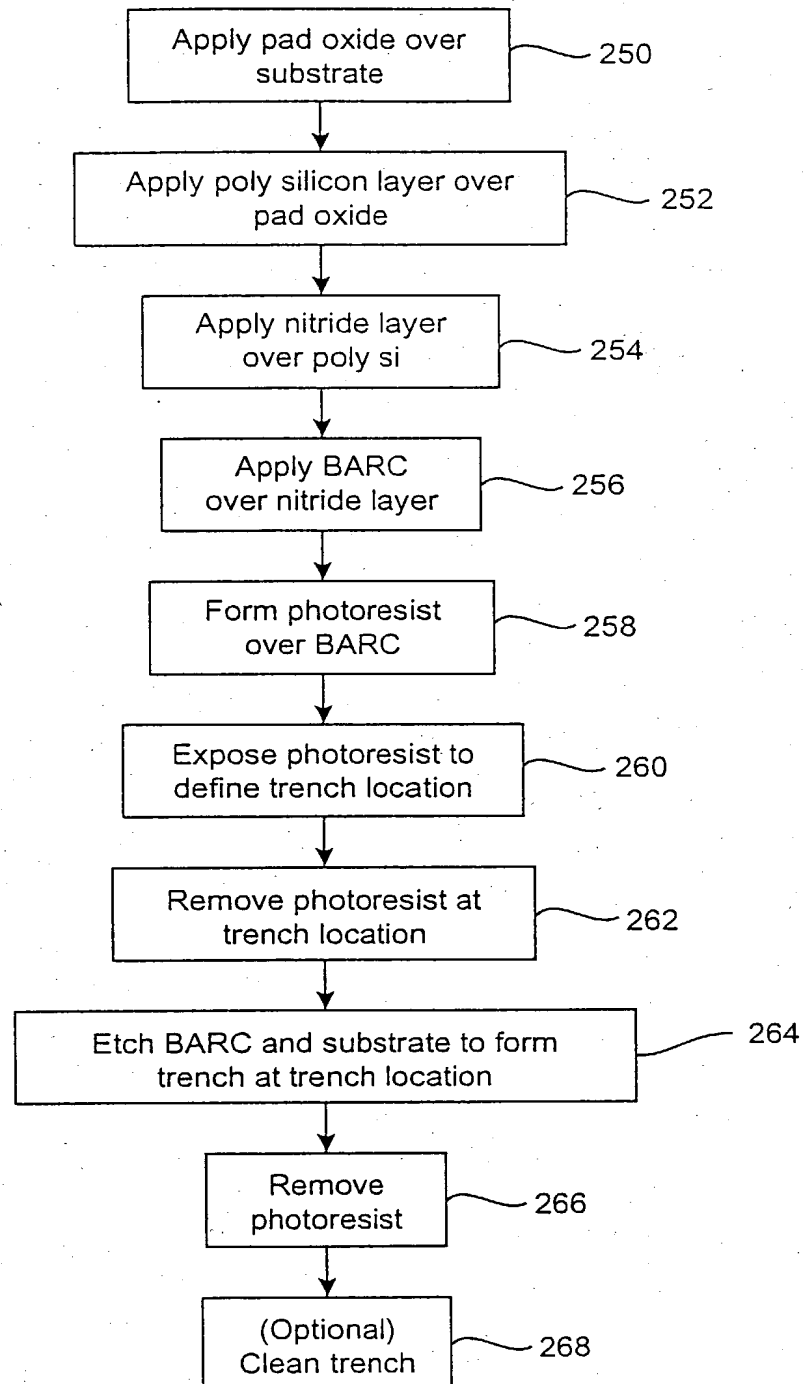


FIG. 3B

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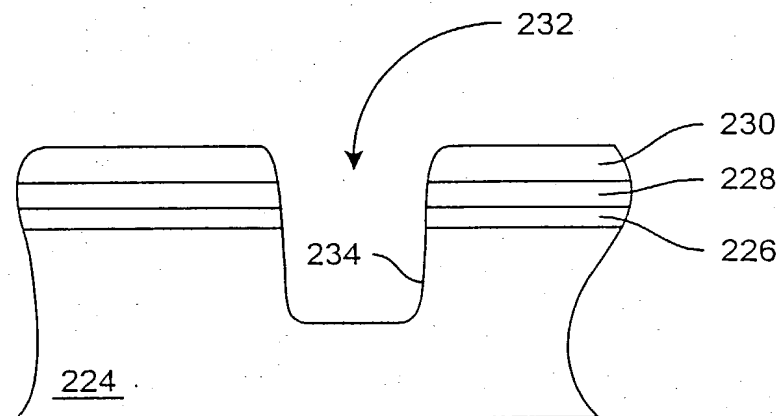


FIG. 4A

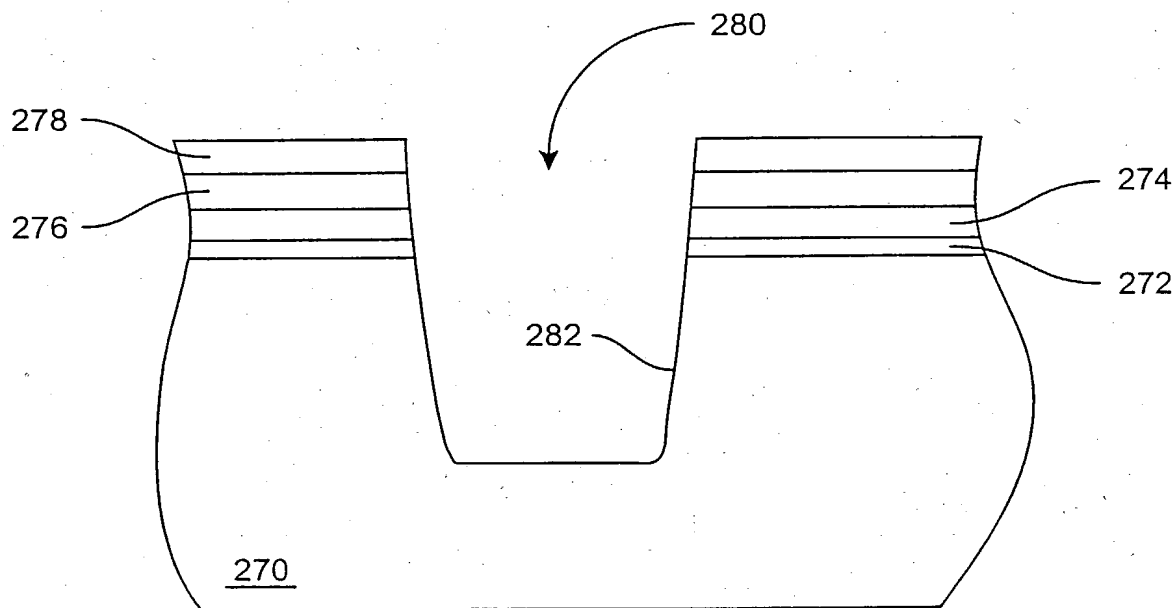


FIG. 4B

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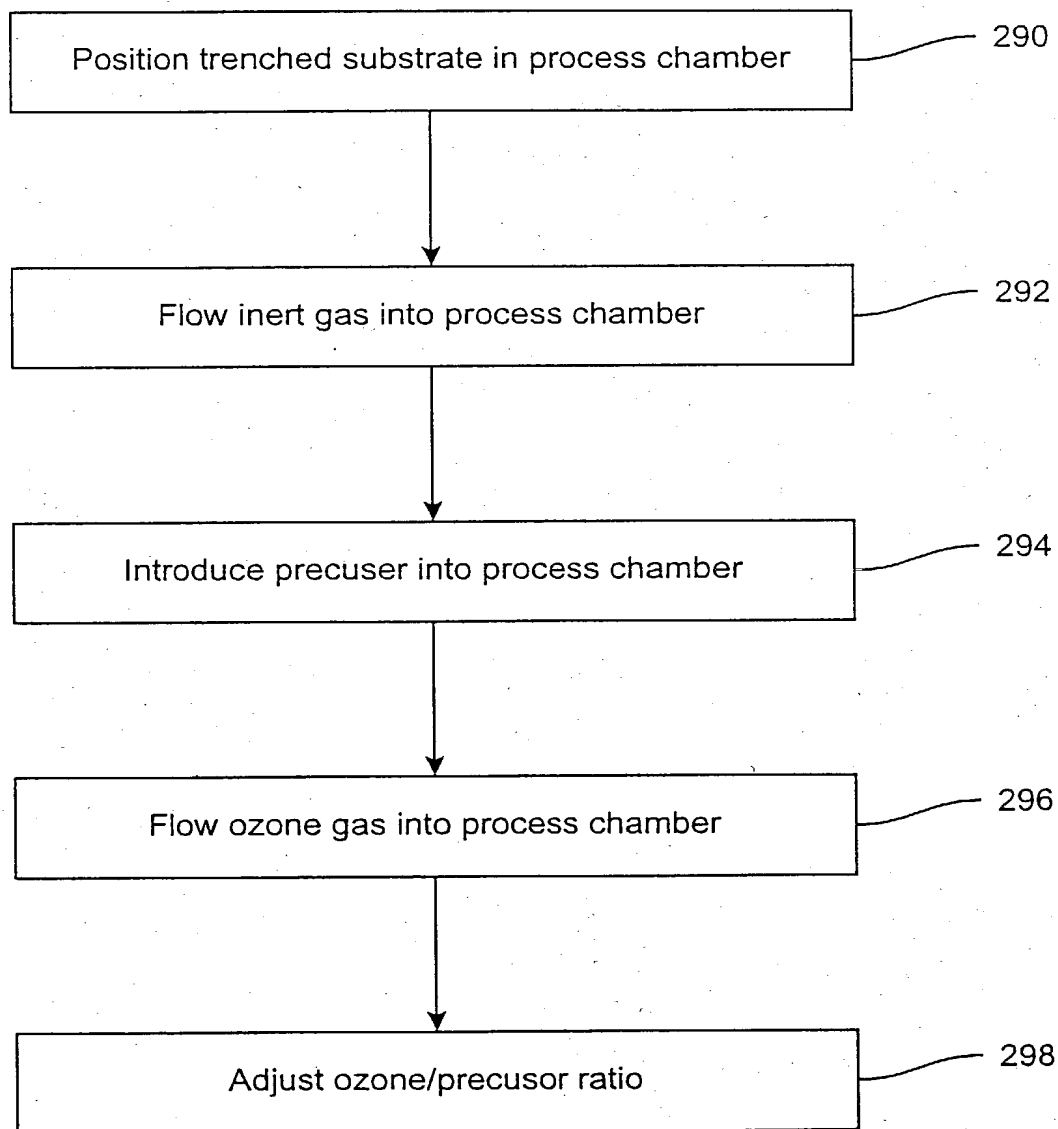


FIG. 5

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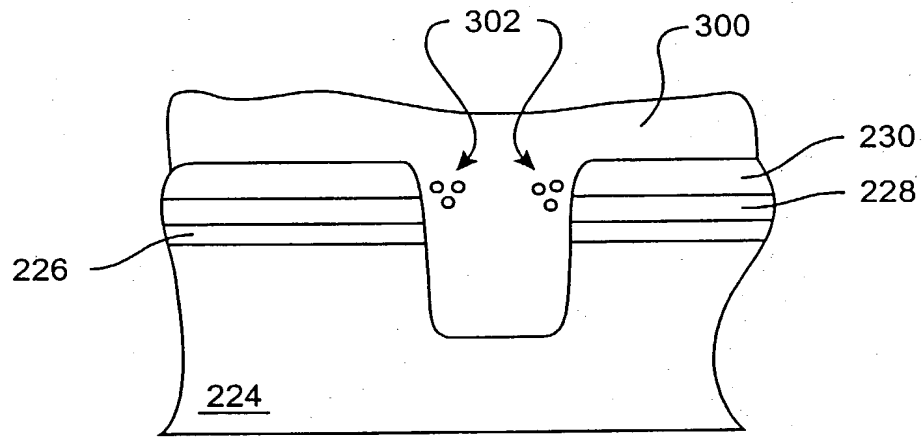


FIG. 6A

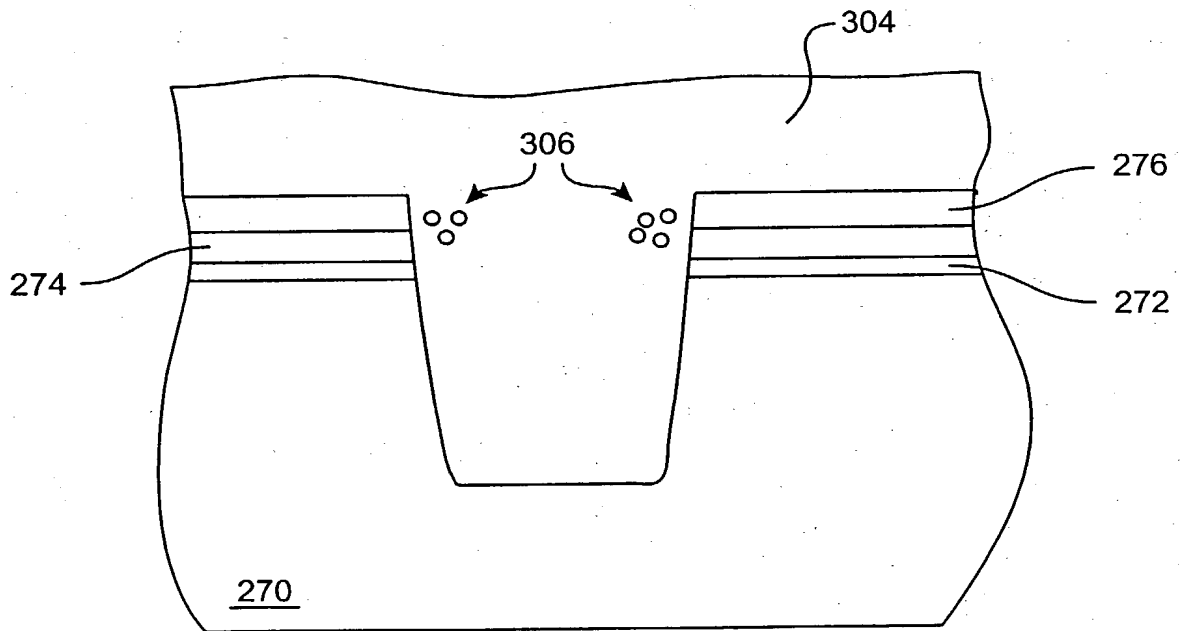


FIG. 6B

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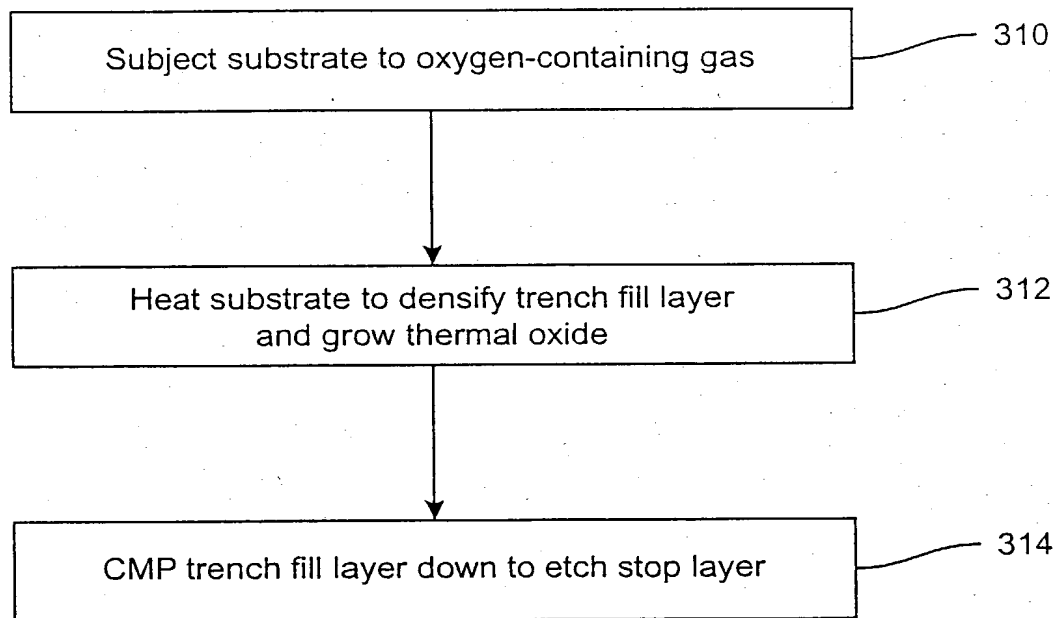


FIG. 7

10 / 15

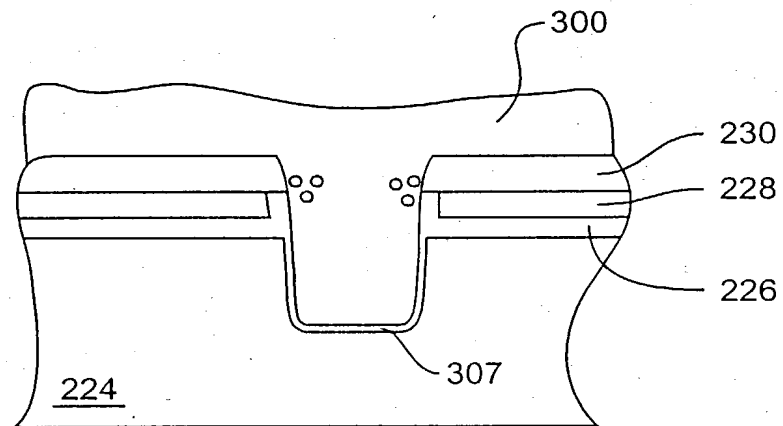


FIG. 8A

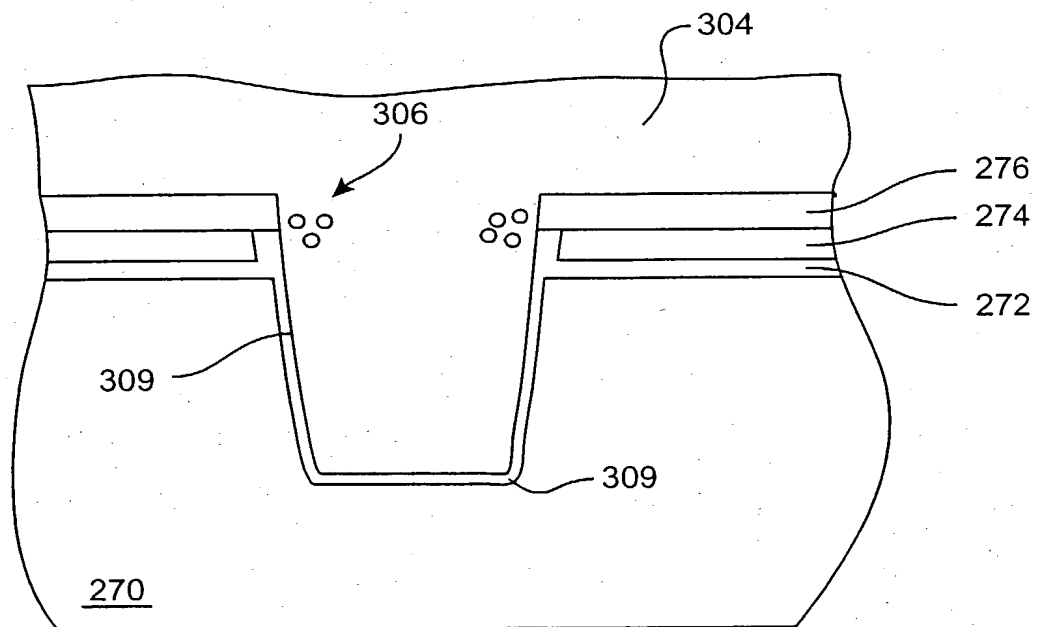


FIG. 8B

11 / 15

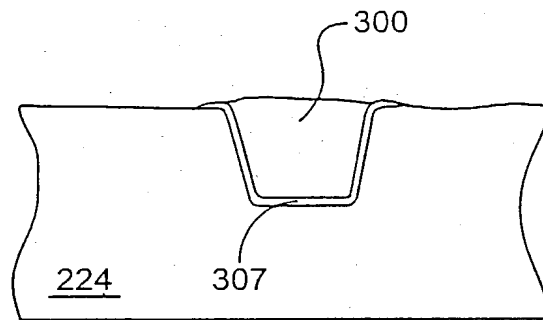


FIG. 9A

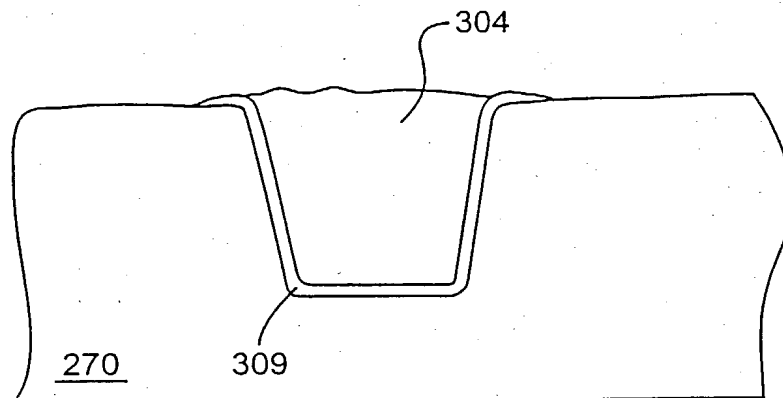
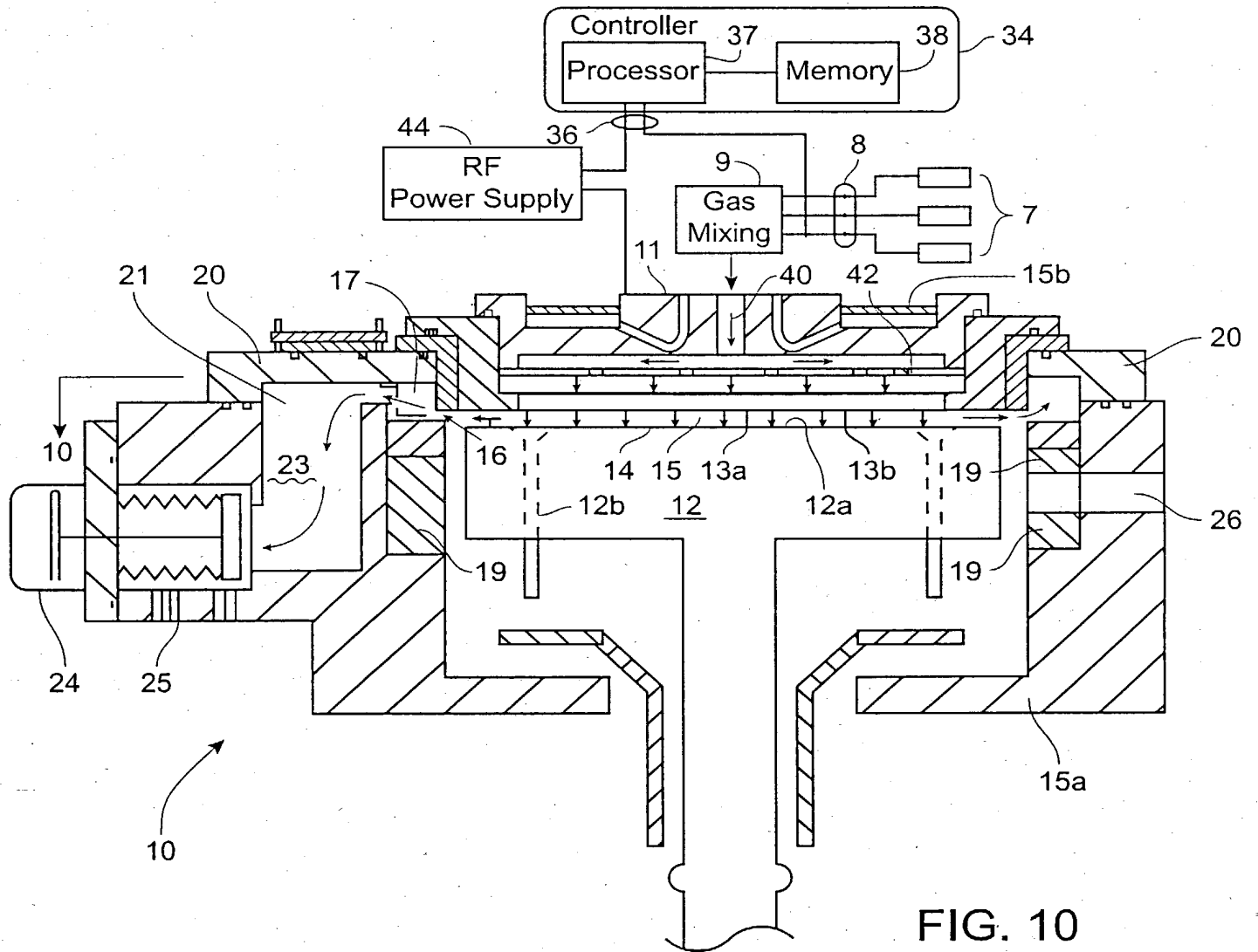


FIG. 9B

12 / 15



13 / 15

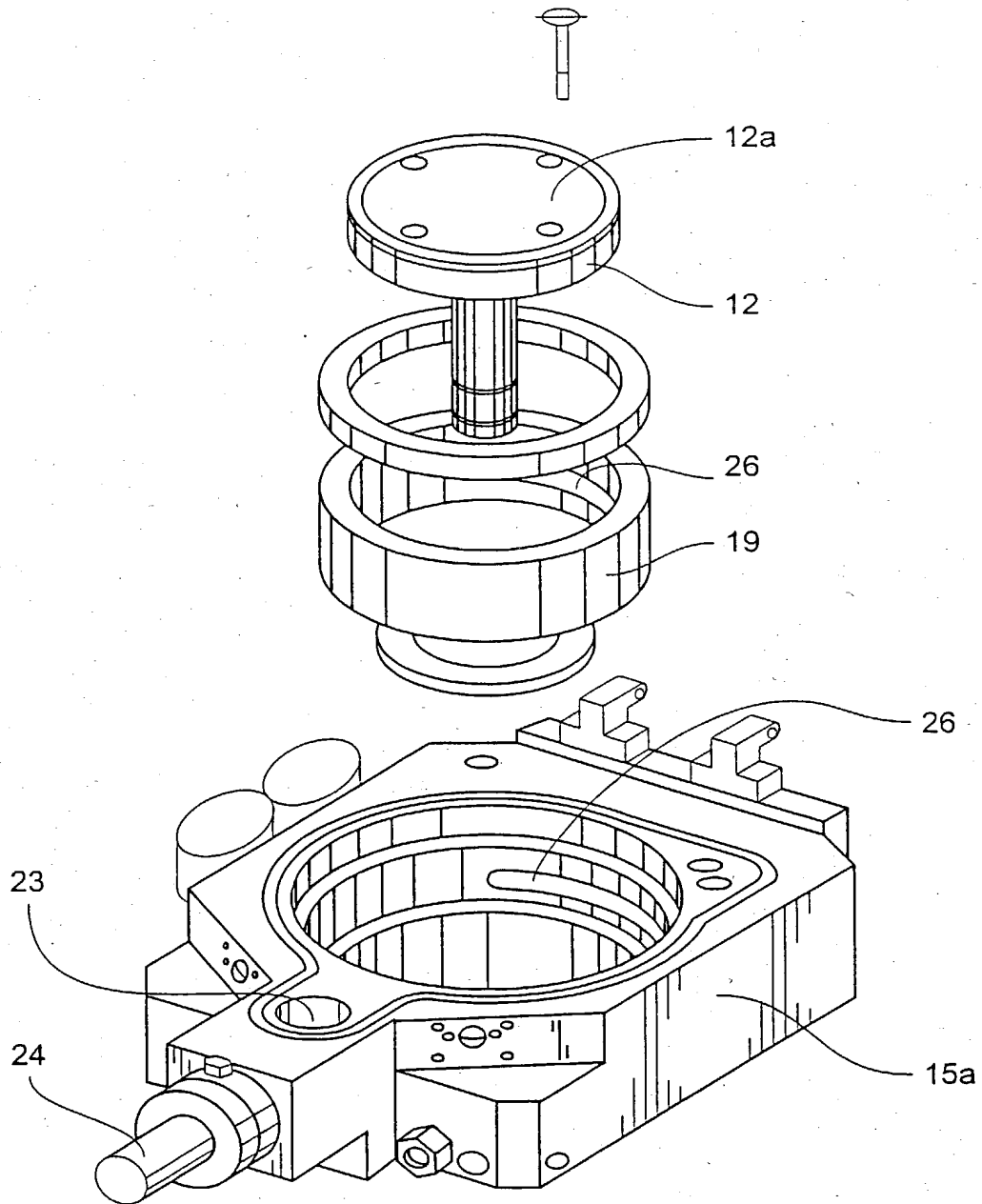
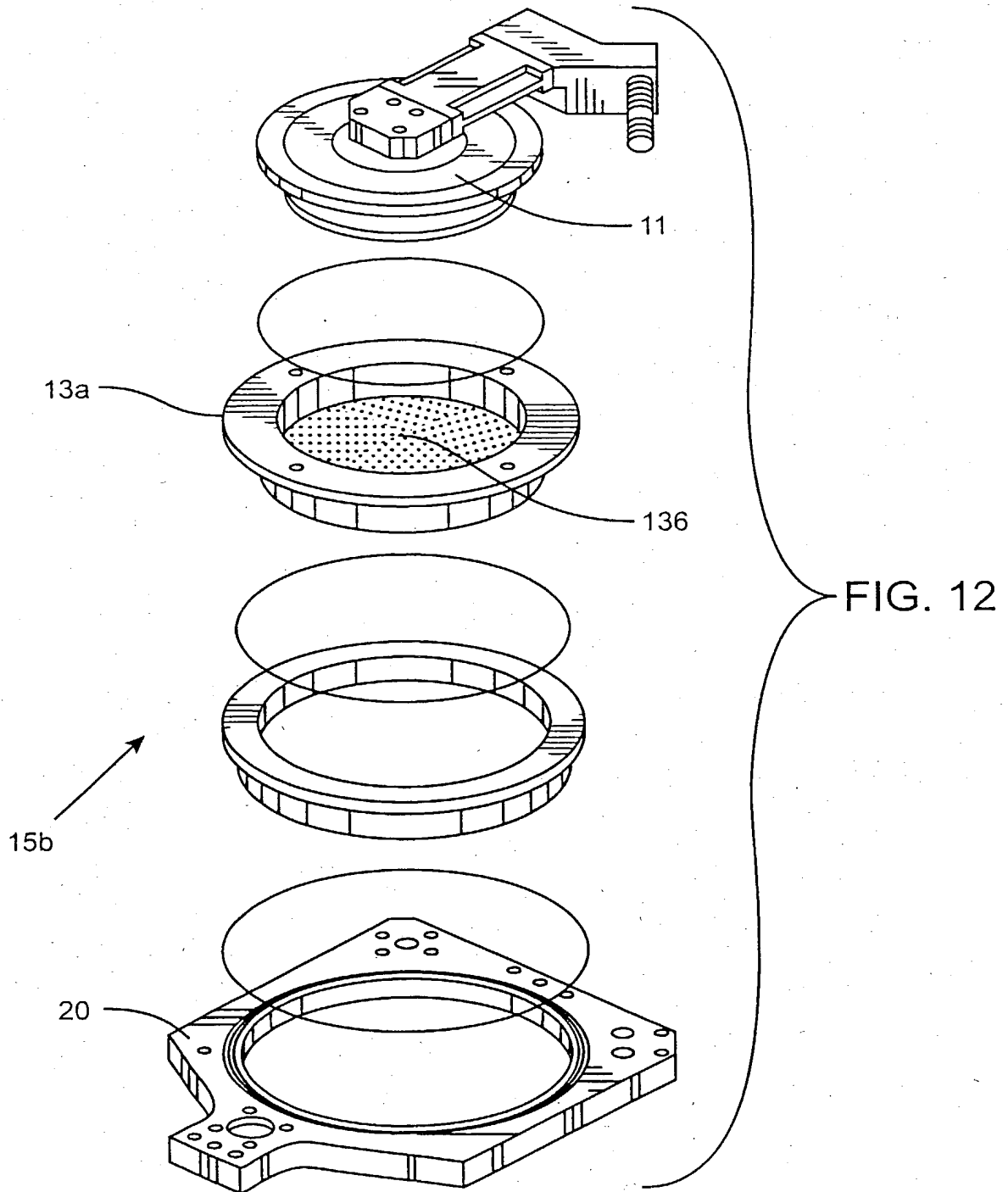


FIG. 11

14 / 15



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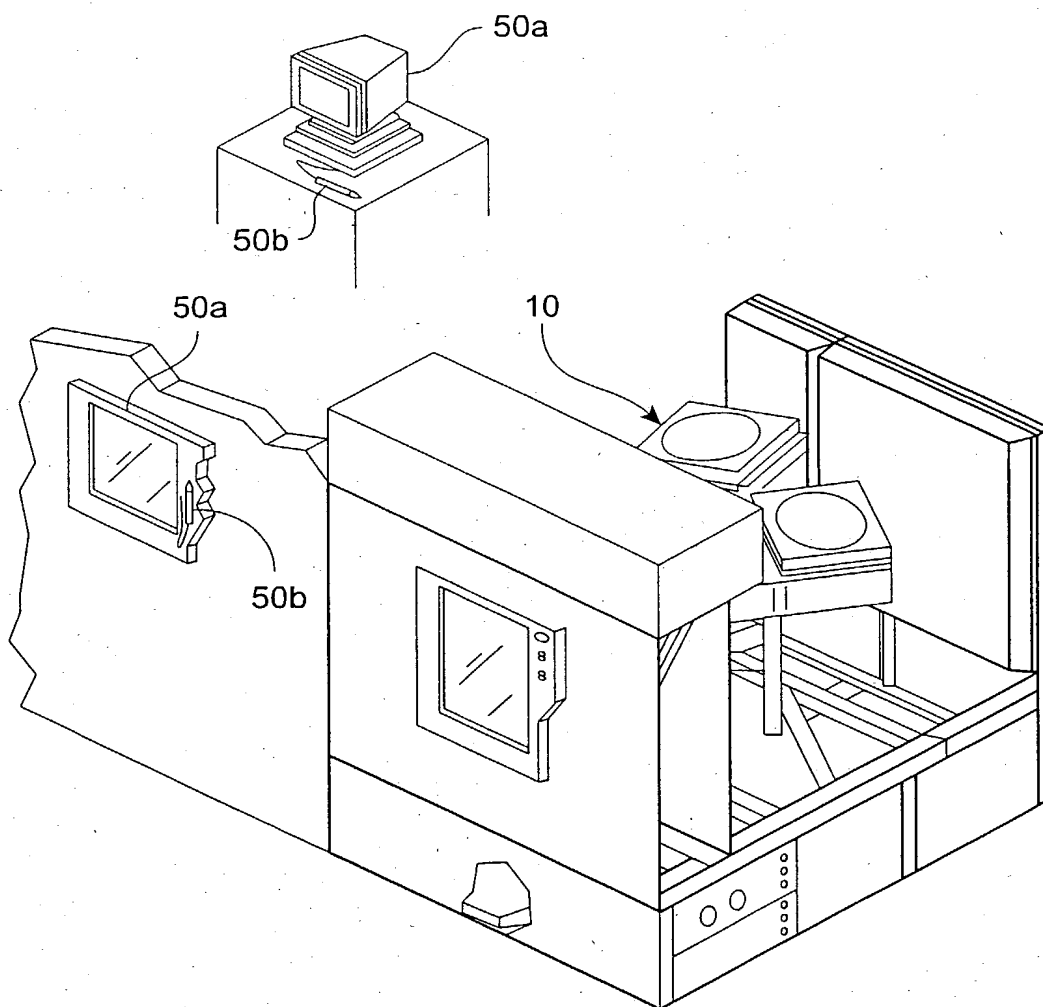


FIG. 13

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

This declaration is of the following type:

- ☒ original
- ☐ divisional
- ☐ continuation
- ☐ continuation-in-part

INVENTORSHIP IDENTIFICATION

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTEGRATION SCHEME USING SELF-PLANARIZED DIELECTRIC LAYER FOR SHALLOW TRENCH ISOLATION

The specification of which:

- ☐ filed herewith;
- ☒ was filed on August 16, 2000, under Serial No. 10/049,689, executed on even date herewith; or
- ☐ Express Mail No. _____ (Serial No. not yet known)
and was amended on _____ (if applicable)
- ☐ was described and claimed in PCT International Application No. _____ filed on _____
and as amended under PCT Article 19 on _____.

ACKNOWLEDGMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56, and which is material to the examination of this application; namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

- ☐ In compliance with this duty there is attached an Information Disclosure Statement in accordance with 37 CFR §1.98.

PRIORITY CLAIM (35 U.S.C. §119)

I hereby claim foreign priority benefits under Title 35, United States Code, §119, of any provisional or foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below, and have also identified below any provisional or foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

- ☐ No such applications have been filed.
- ☒ Such applications have been filed as follows:

PATENT
3299/TCG/PMD

- A. Prior foreign/PCT application(s) filed within 12 mos. (6 mos. for design) prior to this application, and any priority claims under 35 U.S.C. §119

<u>Country/PCT</u>	<u>Application No</u>	<u>Date Filed</u>	<u>Priority Claimed</u>
PCT	US00/22561	8/16/00	[X] Yes [] No
			[] Yes [] No
			[] Yes [] No

- B. All foreign application(s), if any, filed more than 12 mos. (6 mos for design) prior to this U.S. application

Country:
Application No:
Filing date:

- C. U.S. Provisional Application filed within 12 months prior to this application

<u>Serial No.</u>	<u>Filing Date</u>

PRIORITY CLAIM (35 U.S.C. §120)

I hereby claim the benefit under Title 35, United States Code, Section 120, of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose information that is material to the examination of this application (namely, information where there is substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

[X] No such applications have been filed
[] Such application have been filed, as follows:

<u>Serial No.</u>	<u>Filing Date</u>	<u>Status</u>
		<u>Patented</u> <u>Pending</u> <u>Abandoned</u>

POWER OF ATTORNEY

I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

18
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DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Sec. 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

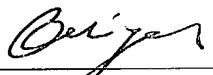
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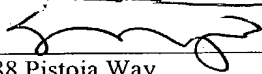
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